Rec. 6/24/02

VERSION WITH MARKINGS TO SHOW CHANGES MADE

25. (Seven times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one activated, annealed p-type area within said at least one n-well and at least one activated, annealed n-type area within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

33. (Five times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one activated, annealed doped area within at least one of said at least one n-well and said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

39. (Five times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one activated, annealed first doped area on said substrate first surface;

at least one activated, annealed second, differently doped area within said at least one first doped area; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

46. (Three times amended) An intermediate structure useful in the formation of electrical device isolation structures, comprising:

a semiconductor substrate having at least a portion that is free of field oxide structures and includes a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well defined on said first surface of said substrate;

at least one activated, annealed p-type area defined within said at least one n-well and at least one activated, annealed n-type area defined within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.